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## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention generally relates to an arbitration method of a bus bridge and, more particularly, to an arbitration method performed by a bus bridge such as a PCI-PCI bridge of personal computers, a PCI-card bus bridge, a PCI-IEEE1394 (OHCI-Link) bridge, etc.

### 2. Description of the Related Art

The performance of computers has been accelerated every year, and peripheral devices such as memory devices are sped up and upgraded. The interface used for the computers and the peripheral devices includes the IEEE1394 interface. The IEEE1394 interface is standardized as a high-speed serial bus for the next generation's multimedia by IEEE, which can be extended over the consumer and the computer.

In the IEEE1394 standard, a data transfer rate from 100 Mbps to 400 Mbps is used. The IEEE1394 allows use of an isochronous transfer so as to guarantee a real-time operation using the isochronous transfer. That is, because the priority right is assigned each 125  $\mu$ s in the isochronous transfer of IEEE1394, the real time operation for the data transfer can be guaranteed.

The above-mentioned IEEE-1394 standard is not

for I/O devices but for buses. When the IEEE-1394  
standard is used for a system, a bus bridge is provided  
so as to interface a primary side bus with a secondary  
side bus, the primary side bus being a local bus in the  
5 system.

There might be a case in which only a limited  
number of bus bridges can be provided in a system, and  
the number of buses to be connected in the system is  
greater than the limited number of bus bridges. In such  
10 a case, two or more buses may be connected to a single  
bus bridge by adding a unique ID to each of the buses.

There is a bridge device that interfaces a  
primary side bus, which is a local bus in the system,  
with a secondary side bus. Such a bridge device may  
15 supports different operations with respect to the bus  
control. For instance, one of the operations relates to  
the serial bus according to the IEEE1394 standard and  
the other operation relates to the bus according to a  
standard other than the IEEE1394 standard.

When the bus in accordance with the IEEE1394  
standard begins accessing the primary side bus, it takes  
a relatively long time to transfer data. Therefore, the  
IEEE1394 bus occupies the access right. Moreover, when  
arbitration is performed, the access right might not be  
25 handed over to other secondary side buses when priority

is given to the IEEE1394 side.

SUMMARY OF THE INVENTION

It is a general object of the present  
5 invention to provide an arbitration method of a bus  
bridge in which the above-mentioned problems are  
eliminated.

A more specific object of the present  
invention is to provide an arbitration method of a bus  
10 bridge which equally gives an access right to secondary  
side buses when the secondary side buses include the  
IEEE1394 bus so that the secondary side buses other than  
the IEEE1394 bus is prevented from being not given the  
access right.

15 In order to achieve the above-mentioned  
objects, there is provided according to one aspect of  
the present invention an arbitration method of a bus  
bridge which interfaces a primary side bus with a  
plurality of secondary side buses, the primary side bus  
20 being a local bus in a system and the secondary side  
buses being external buses connected to the system, the  
bus bridge supporting a plurality of kinds of operations  
one of which is an operation related to a serial bus in  
accordance with IEEE1394, the arbitration method  
25 comprising the step of giving an access right

5 secondary side buses.

10                   In one embodiment, one of the secondary side buses may be the serial bus in accordance with IEEE1394, and the rest of the secondary side buses may be card buses.

Accordingly, when the serial bus in accordance with IEEE1394 is given an access right, an operation with respect to the serial bus in accordance with IEEE1394 can be completed without interruption even if an access demand is lodged from other secondary buses

since the access right is not transferred from the  
serial bus in accordance with IEEE1394 to other  
secondary buses. Thus, the operation of the serial bus  
in accordance with IEEE1394 is prevented from being  
5 failed.

In the arbitration method according to the  
present invention, the secondary side buses may include  
a plurality of card buses, and the arbitration method  
may comprise the steps of: performing an arbitration  
10 between the serial bus in accordance with IEEE1394 and  
the card buses when access demands are lodged from the  
serial bus in accordance with IEEE1394 and the card  
buses; and performing an arbitration between the card  
buses when an access right is to be given to one of the  
15 card buses. Additionally, the arbitration method may  
further comprise the step of changing an order of giving  
the access right.

When the secondary side buses include the  
serial bus in accordance with IEEE1394 and more than two  
20 card buses, an arbitration circuit becomes complex.  
However, according to the present invention, the  
arbitration circuit can be simplified by dividing the  
operation of arbitration into two steps.

In the above-mentioned structure, there may be  
25 a case in which the access right cannot be given equally

5 efficient arbitration can be achieved in response to a  
condition of the system.

10 the primary side bus lodges an access demand to the  
secondary side buses irrespective of a condition of  
arbitration between the secondary side buses.

According to the above-mentioned invention, the operation of arbitration is prevented from being failed due to a collision of an access from the secondary side buses with an access from the primary side bus. That is, when the arbitration is performed with respect to the secondary side buses, the primary side bus is in an idle state. Accordingly, it is possible that an access from the secondary side buses and a access from the primary side bus are made simultaneously, which may result in an operation error. However, such a problem can be eliminated by giving a highest priority to the primary side bus when the primary side bus lodges an access demand to the

secondary side buses.

Additionally, there is provided according to another aspect of the present invention an arbitration method of a bus bridge which interfaces a primary side bus with a plurality of secondary side buses, the primary side bus being a local bus in a system and the secondary side buses being external buses connected to the system, the bus bridge supporting a plurality of kinds of operations one of which is an operation related to a serial bus in accordance with IEEE1394, the arbitration method comprising the step of giving a highest priority to the primary side bus when the primary side bus lodges an access demand to the secondary side buses irrespective of a condition of an arbitration between the secondary side buses.

→ According to the above-mentioned invention, the operation of arbitration is prevented from being failed due to a collision of an access from the secondary side buses with an access from the primary side bus. That is, when the arbitration is performed with respect to the secondary side buses, the primary side bus is in an idle state. Accordingly, it is possible that an access from the secondary side buses and a access from the primary side bus are made simultaneously, which may result in an operation error.



5           Other objects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings.

FIG. 1 is a block diagram of a bus bridge according to a first embodiment of the present invention;

FIG. 3 is a block diagram of an arbiter according to the first embodiment of the present invention.

A description will now be given, with reference to FIG. 1, of a first embodiment of the present invention.

FIG. 1 is a block diagram of a bus bridge  
25 according to the first embodiment of the present

5 primary side bus 21. An IEEE1394 bus 22 is connected to  
an IEEE1394 block 35 provided in the bus bridge 3. The  
bus bridge 3 is also provided with two card-bus blocks  
33 and 34 which have card slots A and B, respectively so  
that a card bus 23A is inserted into the card slot A and  
10 a card bus 23B is inserted into the card slot B. The  
IEEE1394 bus and the card buses 23A and 23b correspond  
to the secondary side buses.

15 The IEEE1394 block 35 performs a bus controlling  
operation in accordance with the IEEE 1394 protocol, and  
also serves as an interface of the IEEE1394 bus.  
Accordingly, the bus bridge 3 shown in FIG. 1 supports  
both the PCI-card bus bridge function and the PCI-1394  
20 (OHCI-Link) bridge function.

25           A bus slave 31 and a bus master 32 are

provided in the bus bridge 3. The data and address of the primary-side buses 21 are given from the bus slave 31 to the secondary-side bus. The data and address of the secondary-side buses 21 are given to the primary-side bus through the bus master 32. The data given to the primary-side bus 21 through the bus master 32 is taken by a host 1 through the bus slave 11. When an access demand CREQQ# is given from the card buses 23A and 23B, each of the card bus blocks 33 and 34 takes the access demand by the internal slave provided therein, and gives the access right to the arbiter 36. The arbiter 36 performs arbitration as described later, and outputs the acknowledgement ACK to the permitted card-bus block. The card-bus blocks 33 and 34 give enabling signal CGNT # from the master thereof to the card bus 23A or 23B based on the acknowledgement ACK obtained from the arbiter 36.

The card bus 23A and 23B give the address and data to the respective bus blocks 33 and 34 based on an enabling signal CGNT#. Then, the bus blocks 33 and 34 send the address and data to the primary side bus 21 through the bus master 32.

When the access demand REQ1394 is given from the 1394(PHY) bus 22, the IEEE1394 block 35 outputs the access demand REQ1394 to the arbiter 36. When

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If a priority is given to the IEEE1394 bus 22, which occupies the primary-side bus 21 for a long time, there may be a case in which the access right cannot be transferred to the card buses 23A and 23B or probability  
5 of transferring the access right to the card buses 23A and 23B is extremely lowered, which prevents a normal data transfer.

When more than two access demands REQs are supplied at the same time, a priority is not given to  
10 the IEEE1394 block 35, and the access right is given equally at the same rate with other blocks. Therefore, the arbiter 36 is provided with a counter so as to give the access right sequentially to the buses that have lodged the access demands REQs.

15 As a result, the acknowledgement ACK is supplied to the secondary-side buses equally at the same rate. Therefore, the access right is given sequentially to the secondary-side buses, and the arbiter 36 does not need a special circuit.

20 When the access right is given to the IEEE1394 bus 22 and when an operation is being performed through the IEEE1394 bus, the operation cannot be stopped due to the feature of the operation according to IEEE1394 until the operation according to the IEEE1394 is completed  
25 even if the access demand REQ is supplied from the card

bus 23A or 23B.

Accordingly, when the IEEE1394 bus 22 is busy, the arbiter 36 is prevented from taking up the access right from the IEEE1394 bus 22. This can be achieved by inputting a busy signal representing the busy state of the IEEE1394 bus 22 to the arbiter 36 so as to monitor the busy signal by the arbiter 36. However, in the present embodiment, the busy signal representing the busy state of the IEEE1394 bus 22 is reflected in the access demand REQ. Specifically, the access demand IEEE1394 is lowered when the busy signal falls, and sequentially, the acknowledgement ACK1394 is lowered when the busy signal falls. Accordingly, the acknowledgement ACK1394 is continuously supplied until the access demand REQ1394 is withdrawn. Thus, when the IEEE1394 bus is busy, the access right given to the IEEE1394 bus 22 is not taken up without increasing the number of inputs to the arbiter 36.

Since each of the card buses 23A and 23B is an isolated bus besides the IEEE1394 bus 22, the acknowledgement ACK can be sent back to the card buses 23A and 23B. However, because the use right of the primary-side bus 21 is not given to the card buses 23A and 23B, the card buses 23A and 23B cannot transfer data. Therefore, it is necessary to make the card buses 23A

and 23B to send the access demand again.

When the card bus is used as the secondary-side bus as is in the above-mentioned embodiment, signals CREQ# and CGNT# corresponding to the access demand REQ and the acknowledgement ACK, respectively, are input. Thus, the signals CREQ# and CGNT# may be input to the arbiter 36 instead of inputting the access demand REQ and the acknowledgement ACK. However, it should be noted that a car has to be taken since the polarities of the low and high levels are reversed.

When the number of agents who lodge the access demand REQ is greater than three as in the above-mentioned embodiment, the circuit structure of the bus bridge 3 becomes complex. In order to simplify the circuit structure, the arbiter 36 is divided into two stages of a first arbiter 36a and a second arbiter 36b as shown in FIG. 3. The first arbiter 36a performs the arbitration of the access demands of the IEEE1394 bus 22 and the card buses 23A and 23B. The second arbiter 32b performs the arbitration of the access demands of the card buses 23A and 23B only at a time when Card-ACK is returned.

According to the above-mentioned structure of the arbiter 36, each of the arbiter 36a and 36b merely performs the selection of one from two. Therefore, the

first arbiter 36a and the second arbiter 36b can be composed of the same circuit. At this time, Card-REQ can be simply generated by an OR operation of REQ-A and REQ-B.

5                   However, according to the above-mentioned structure, the access right cannot be given to the three agents equally. Specifically, in the above-mentioned embodiment, the ratio of slot A : slot B : IEEE1394 becomes equal to the ratio 1 : 1 : 2.

10                   Although some systems allow such a distribution of the access right, when a completely equalized distribution of the access right is desired, the distribution ratio of the first arbiter 36a must be such that the ratio of card bus to the IEEE1394 bus  
15 (card bus : IEEE1394) must be equal to 2 : 1. In order to achieve this scheme, a switch bit is merely provided to the internal register of the bus bridge. Moreover, there is no need to make a special arbitration circuit. For example, the arbitration circuit may give the access  
20 right to the IEEE1394 bus after giving the access right to the card buses twice.

                  In the above-mentioned bus bridge 3, malfunction may occur due to a collision on the primary-side bus when the access from the secondary-side bus is  
25 accepted during the arbitration of the secondary-side



buses. In such a case, the access of the primary-side bus should not be retried (canceling the access without accepting the access at that time, and the same access is reissued later), and the current access of the

5 primary-side bus should be given a highest priority.

The reason for this is not to be able to give priority to the access of the secondary-side bus because it is uncertain what process is done by the bus master of the primary-side bus.

10 As for the operation of the arbiter 36, it is ideal not to return the acknowledge ACK to the secondary-side bus. However, there may be a case in which the arbiter has already sent the acknowledgement ACK to the card busses. In such a case, the card buses  
15 are rendered to send the access demand again.

Alternatively, the access of the secondary-side bus can be accepted by setting separate paths to the process of the data path of the primary side and the data path of the secondary side.

20 However, since the primary-side bus is not in an idle state, the data to be transferred must be held in the bus master 2 of the bus bridge 3. In the case of the IEEE1394 bus, since the retry cannot be done on the secondary side, the access from the primary side is an  
25 access to the internal register. Thus, there is no need

It should be noted that the present invention can be applied also to the USB as a similar serial bus in accordance with IEEE1394.

The present invention is based on Japanese  
0 priority application filed on July 5, 1999, the entire  
contents of which are hereby incorporated by reference.

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